Claims

[c1] What is claimed is:

1.A method for programming a single-bit storage SONOS memory cell, wherein said single-bit storage SONOS memory cell comprises a channel region between a left bit line and a right bit line, a composite dielectric layer for storing digital data, and a word line overlying said composite dielectric layer, the method comprising: performing a left side electron injection on said single-bit storage SONOS memory cell by applying a relatively high word line voltage ($V_{WL, HIGH}$) to said word line, applying a relatively high left bit line voltage ($V_{LBL, HIGH}$) to said left bit line, and applying a relatively low right bit line voltage ($V_{RBL, LOW}$) to said right bit line; and performing a right side electron injection on said single-bit storage SONOS memory cell by applying said relatively high word line voltage ($V_{WL, HIGH}$) to said word line, applying a relatively low left bit line voltage ($V_{LBL, LOW}$) to said left bit line, and applying a relatively high right bit line voltage ($V_{RBL, HIGH}$) to said right bit line.

[c2] 2.The method according to claim 1 wherein said composite dielectric layer is an ONO tri-layer dielectric in-

cluding a bottom silicon oxide layer, a middle silicon nitride layer, and a top silicon oxide layer.

[c3] 3.The method according to claim 1 wherein said left bit line and said right bit line are both buried bit lines that are implanted into a substrate.

[c4] 4.A method for programming a single-bit storage nonvolatile memory cell, comprising:
providing a single-bit storage nonvolatile memory cell comprising a channel region between a left bit line and a right bit line, a composite dielectric layer for storing digital data, and a word line overlying said composite dielectric layer;
performing a left side electron injection on said single-bit storage nonvolatile memory cell by applying a relatively high word line voltage ($V_{WL, HIGH}$) to said word line, applying a relatively high left bit line voltage ($V_{LBL, HIGH}$) to said left bit line, and applying a relatively low right bit line voltage ($V_{RBL, LOW}$) to said right bit line; and
performing a right side electron injection on said single-bit storage nonvolatile memory cell by applying said relatively high word line voltage ($V_{WL, HIGH}$) to said word line, applying a relatively low left bit line voltage ($V_{LBL, LOW}$) to said left bit line, and applying a relatively high right bit line voltage ($V_{RBL, HIGH}$) to said right bit line.

[c5] 5.The method according to claim 4 wherein said single-bit storage nonvolatile memory cell is a single-bit storage SONOS memory cell.

[c6] 6.The method according to claim 4 wherein said composite dielectric layer is an ONO tri-layer dielectric including a bottom silicon oxide layer, a middle silicon nitride layer, and a top silicon oxide layer.